We Claim:

1. A semiconductor structure comprising:

a monocrystalline substrate;

a monocrystalline accommodating buffer layer overlying said monocrystalline substrate, wherein said monocrystalline accommodating buffer layer is formed of a monocrystalline oxide that is exposed to a concentration of niobium while being deposited overlying said monocrystalline substrate; and

a monocrystalline compound semiconductor material layer overlying said monocrystalline accommodating buffer layer.

2. The semiconductor structure of claim 1, wherein said concentration of niobium is kept constant while said monocrystalline oxide is deposited overlying said monocrystalline substrate.

3. The semiconductor structure of claim 1, wherein said concentration of niobium is increased as said monocrystalline oxide is deposited overlying said monocrystalline substrate.

4. The semiconductor structure of claim 1, said monocrystalline compound semiconductor material layer comprising a material selected from one of: Group III-V compound semiconductors, mixed III-V compound semiconductors, Group II-VI compound semiconductors, mixed II-VI compound semiconductors, Group IV-VI compounds semiconductors, and mixed IV-VI compound semiconductors.

5. The semiconductor structure of claim 1, wherein said monocrystalline compound semiconductor material layer comprises a material selected from at least one of: gallium arsenide, gallium aluminum arsenide, gallium indium arsenide, indium phosphide, cadmium sulfide, cadmium mercury telluride, zinc selenide, zinc sulfur selenide, lead selenide, lead telluride, and lead sulfide selenide.

6. The semiconductor structure of claim 1, wherein said monocrystalline oxide comprises a material selected from at least one of: alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal vanadates, perovskite

oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

7. The semiconductor structure of claim 1, further comprising a template layer formed overlying said accommodating buffer layer and underlying said monocrystalline compound semiconductor material layer.

8. The semiconductor structure of claim 7, wherein said template layer comprises a Zintl-type phase material.

9. The semiconductor structure of claim 7, wherein said template layer comprises a surfactant material.

10. The semiconductor structure of claim 9, wherein said template layer further comprises a capping layer.

11. The semiconductor structure of claim 10, wherein said capping layer is formed by exposing said surfactant material to a cap-inducing material.

12. The semiconductor structure of claim 7, wherein said template layer comprises a capping layer formed of about 1-10 monolayers of one of a material M-N and a material M-O-N, wherein M is selected from at least one of Zr, Hf, Sr, Ti, and Ba and N is selected from at least one of As, P, Ga, Al, and In.

13. The semiconductor structure of claim 1, wherein said monocrystalline accommodating buffer layer is formed of a monocrystalline material and is subsequently heat treated to convert at least a portion of said monocrystalline material to an amorphous material.

14. The semiconductor structure of claim 1, further comprising an amorphous interface layer overlying said monocrystalline substrate and underlying said monocrystalline accommodating buffer layer.

15. The semiconductor structure of claim 1, said monocrystalline substrate comprising silicon.

16. The semiconductor structure of claim 2, wherein said accommodating buffer layer comprises $SrTi_{0.44}Nb_{0.56}O_3$.

17. The semiconductor structure of claim 3, wherein said accommodating buffer layer comprises $SrTi_{1-x}Nb_xO_3$, where x increases from about zero to about 0.56 as said accommodating buffer layer is deposited overlying said monocrystalline substrate.

18. The semiconductor structure of claim 1, said accommodating buffer layer having thickness of from about 2 to about 100 nanometers.

19. A semiconductor structure comprising:

a monocrystalline substrate having a first lattice constant;

a monocrystalline accommodating buffer layer overlying said monocrystalline substrate, wherein upon proper orientation said monocrystalline accommodating buffer layer has a second lattice constant proximate to said monocrystalline substrate, said second lattice constant substantially matched to said first lattice constant; and

a monocrystalline compound semiconductor material layer overlying said monocrystalline accommodating buffer layer, said monocrystalline compound semiconductor material layer having a third lattice constant,

wherein said monocrystalline accommodating buffer layer is formed of a monocrystalline oxide which is exposed to a concentration of niobium while being deposited overlying said monocrystalline substrate such that said monocrystalline accommodating buffer layer has a fourth lattice constant proximate to said monocrystalline compound semiconductor material layer, said fourth lattice constant being substantially matched to said third lattice constant.

20. The semiconductor structure of claim 19, said monocrystalline compound semiconductor material layer comprising a material selected from one of: Group III-V compound semiconductors, mixed III-V compound semiconductors, Group II-VI compound semiconductors, mixed II-VI compound semiconductors, Group IV-VI compound semiconductors, and mixed IV-VI compound semiconductors.

21. The semiconductor structure of claim 19, wherein said monocrystalline compound semiconductor material layer comprises a material selected from at least one of: gallium arsenide, gallium aluminum arsenide, gallium indium arsenide, indium phosphide, cadmium sulfide, cadmium mercury telluride, zinc selenide, zinc sulfur selenide, lead selenide, lead telluride, and lead sulfide selenide.

22. The semiconductor structure of claim 19, wherein said monocrystalline accommodating buffer layer comprises a material selected from at least one of: alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal

vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

23. The semiconductor structure of claim 19, wherein said monocrystalline substrate comprises silicon.

24. The semiconductor structure of claim 23, wherein said monocrystalline compound semiconductor material layer comprises GaAs and said monocrystalline accommodating buffer layer comprises $SrTi_{1-x}Nb_xO_3$, where x increases from about zero proximate to said monocrystalline substrate to about 0.56 proximate to said monocrystalline compound semiconductor material layer.

25. The semiconductor structure of claim 19, further comprising a template layer formed overlying said accommodating buffer layer and underlying said monocrystalline compound semiconductor material layer.

26. The semiconductor structure of claim 25, wherein said template layer comprises a Zintl-type phase material.

27. The semiconductor structure of claim 25, wherein said template layer comprises a surfactant material.

28. The semiconductor structure of claim 27, wherein said template layer further comprises a capping layer.

29. The semiconductor structure of claim 28, wherein said capping layer is formed by exposing said surfactant material to a cap-inducing material.

30. The semiconductor structure of claim 25, wherein said template layer comprises a capping layer formed of about 1-10 monolayers of one of a material M-N and a material M-O-N, wherein M is selected from at least one of Zr, Hf, Sr, Ti, and Ba and N is selected from at least one of As, P, Ga, Al, and In.

31. The semiconductor structure of claim 19, wherein said monocrystalline accommodating buffer layer is formed of a monocrystalline material and is subsequently heat treated to convert at least a portion of said monocrystalline material to an amorphous material.

32. The semiconductor structure of claim 19, further comprising an amorphous interface layer overlying said monocrystalline substrate and underlying said monocrystalline accommodating buffer layer.

33. A process for fabricating a semiconductor structure, the process comprising:

providing a monocrystalline substrate;

forming a monocrystalline accommodating buffer layer overlying said monocrystalline substrate by depositing a monocrystalline oxide overlying said monocrystalline substrate while exposing said monocrystalline oxide to a concentration of niobium during at least a portion of said depositing, said monocrystalline accommodating buffer layer terminating in a material having a first lattice constant; and

epitaxially forming a monocrystalline compound semiconductor material layer overlying said monocrystalline accommodating buffer layer, said first lattice constant being substantially matched to a lattice constant of said monocrystalline compound semiconductor material layer.

34. The process of claim 33, wherein said monocrystalline oxide has a second lattice constant proximate to said monocrystalline substrate, said second lattice constant being substantially matched to a lattice constant of said monocrystalline substrate.

35. The process of claim 33, wherein said concentration of niobium is substantially constant during said exposing.

36. The process of claim 33, wherein said concentration of niobium is increased during said exposing.

37. The process of claim 33, said monocrystalline substrate comprising silicon.

38. The process of claim 33, wherein said accommodating buffer layer comprises $SrTi_{0.44}Nb_{0.56}O_3$.

39. The process of claim 33, wherein said accommodating buffer layer comprises $SrTi_{1-x}Nb_xO_3$, where x increases from about zero proximate to said monocrystalline substrate to about 0.56 proximate to said monocrystalline compound semiconductor material layer.

40. The process of claim 33, said accommodating buffer layer having thickness of from about 2 to about 100 nanometers.

41. The process of claim 33, said monocrystalline compound semiconductor material layer comprising a material selected from one of: Group III-V compound semiconductors, mixed III-V compound semiconductors, Group II-VI compound

semiconductors, mixed II-VI compound semiconductors, Group IV-VI compounds semiconductors, and mixed IV-VI compound semiconductors.

42. The process of claim 33, wherein said monocrystalline compound semiconductor material layer comprises a material selected from at least one of: gallium arsenide, gallium aluminum arsenide, gallium indium arsenide, indium phosphide, cadmium sulfide, cadmium mercury telluride, zinc selenide, zinc sulfur selenide, lead selenide, lead telluride, and lead sulfide selenide.

43. The process of claim 33, wherein said monocrystalline oxide comprises a material selected from at least one of: alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

44. The process of claim 33, further comprising forming a template layer overlying said accommodating buffer layer and underlying said monocrystalline compound semiconductor material layer.

45. The process of claim 44, wherein said forming a template layer comprises capping said monocrystalline accommodating buffer layer with about 1-10 monolayers of a material M-N and a material M-O-N, wherein M is selected from at least one of Zr, Hf, Sr, Ti, and Ba and N is selected from at least one of As, P, Ga, Al, and In.

46. The process of claim 33, further comprising forming an amorphous interface layer between said monocrystalline substrate and said monocrystalline accommodating buffer layer.

47. A semiconductor device structure comprising:

a monocrystalline silicon substrate;

a monocrystalline accommodating buffer layer overlying said monocrystalline silicon substrate, wherein said monocrystalline accommodating buffer layer is formed of a monocrystalline oxide that is exposed to a concentration of niobium while being deposited overlying said monocrystalline substrate;

a monocrystalline compound semiconductor material layer overlying said monocrystalline accommodating buffer layer;

a first semiconductor component, at least a portion of which is formed in said monocrystalline silicon substrate; and

a second semiconductor component, at least a portion of which is formed in said monocrystalline compound semiconductor material layer, said second semiconductor component being electrically coupled to said first semiconductor component.

48. The semiconductor device structure of claim 47, wherein said concentration of niobium is kept constant while said monocrystalline oxide is deposited overlying said monocrystalline substrate.

49. The semiconductor device structure of claim 47, wherein said concentration of niobium is increased as said monocrystalline oxide is deposited overlying said monocrystalline substrate.

50. The semiconductor structure of claim 47, wherein said monocrystalline oxide comprises a material selected from at least one of: alkaline earth metal titanates, alkaline earth metal zirconates, alkaline earth metal hafnates, alkaline earth metal tantalates, alkaline earth metal ruthenates, alkaline earth metal vanadates, perovskite oxides such as alkaline earth metal tin-based perovskites, lanthanum aluminate, lanthanum scandium oxide, and gadolinium oxide.

51. The semiconductor device structure of claim 47, further comprising a template layer formed overlying said accommodating buffer layer and underlying said monocrystalline compound semiconductor material layer.

52. The semiconductor device structure of claim 47, wherein said monocrystalline accommodating buffer layer is formed of a monocrystalline material and is

subsequently heat treated to convert at least a portion of said monocrystalline material to an amorphous material.

53. The semiconductor device structure of claim 47, further comprising an amorphous interface layer overlying said monocrystalline substrate and underlying said monocrystalline accommodating buffer layer.

54. The semiconductor device structure of claim 47, said monocrystalline substrate comprising silicon.

55. The semiconductor device structure of claim 48, wherein said accommodating buffer layer comprises $SrTi_{0.44}Nb_{0.56}O_3$.

56. The semiconductor device structure of claim 49, wherein said accommodating buffer layer comprises $SrTi_{1-x}Nb_xO_3$, where x increases from about zero proximate to said monocrystalline silicon substrate to about 0.56 proximate to said monocrystalline compound semiconductor material layer.

57. The semiconductor device structure of claim 1, said accommodating buffer layer having thickness of from about 2 to about 100 nanometers.